# Abstracts

## Low-loss CPW lines on surface stabilized high-resistivity silicon

*H.S. Gamble, B.M. Armstrong, S.J.N. Mitchell, Y. Wu, V.F. Fusco and J.A.C. Stewart. "Low-loss CPW lines on surface stabilized high-resistivity silicon." 1999 Microwave and Guided Wave Letters 9.10 (Oct. 1999 [MGWL]): 395-397.*

The authors propose a solution to the surface conduction problem in silicon monolithic microwave integrated circuits (MMIC's). An LPCVD polycrystalline silicon layer is deposited over the surface of a high-resistivity silicon wafer which is then covered with a silicon dioxide layer. The polycrystalline silicon layer effectively removes, through traps, any free electrons or holes that may have been induced at the oxide-silicon interface. The CPW lines with 1.25-/spl mu/m aluminum metallization on passivated HRS substrates have an attenuation loss at 30 GHz of only 1.08 dB/cm.

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